Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus adapted to send a plurality of memory transactions over a memory bus to a memory having a plurality of memory banks, the apparatus comprising:

a queue comprising a plurality of request stations, wherein each of ~~storing a~~ the plurality of memory transactions ~~to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction~~ is stored in one of the request stations and is addressed to one of the plurality of memory banks; and

an arbiter simultaneously coupled to each of the ~~plurality of memory transactions~~ plurality of request stations, adapted to select any of the plurality of memory transactions, and configured to:

generate a plurality of bank readiness signals, each bank readiness signal indicating the readiness of one of the plurality of memory banks to accept a memory transaction, and

select one of the plurality of memory transactions for transmission over the memory bus based on the bank readiness signals.

2. (Original) The apparatus of claim 1, further comprising:

a memory controller configured to send the selected memory transaction over the memory bus.

3. (Currently Amended) The apparatus of claim 1, further comprising:

a queue controller configured to associate with each of the memory transactions a different priority in a set of priorities; and wherein

the arbiter is further configured to:

determine that a priority associated with one of the memory transactions is greater than a priority associated with any of the other memory transactions, and

select the one of the memory transactions when the bank readiness signal indicates that the memory bank, to which the one of the memory transactions is destined, is ready to accept ~~a memory transaction associated with~~ the one of the memory transactions ~~is greater than a priority associated with any of the other memory transactions~~.

4. (Original) The apparatus of claim 3, wherein:

each priority represents an age of a memory transaction.

5. (Previously Presented) The apparatus of claim 1, wherein:

the plurality of memory transactions enter the queue at a first request station and progress toward a second request station until selected for transmission over the memory bus based on the bank readiness signals.

6. (Original) The apparatus of claim 1, wherein:

the arbiter is further configured to send a memory transaction to a memory bank, clear the bank readiness signal for the memory bank at approximately the time of sending the memory transaction to the memory bank, and set the bank readiness signal for the memory bank a predetermined period of time after sending the memory transaction to the memory bank.

7. (Currently Amended) A method comprising:

identifying a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks;

generating a ~~plurality of~~ first bank readiness ~~signals~~ signal by monitoring ~~the addresses~~ an address of a first one of the plurality of memory transactions gated across the memory bus at a location along the memory bus, ~~each~~ wherein the first bank readiness signal ~~indicating~~ indicates the readiness of one of the memory banks to accept ~~a~~ the first one of the plurality of memory ~~transaction~~ transactions;

generating a second bank readiness signal by monitoring an address of a second one of the plurality of memory transactions gated across the memory bus at a location along the memory bus, wherein the second bank readiness signal indicates the readiness of another of the memory banks to accept the second one of the plurality of memory transactions; and

selecting a third one of the memory transactions for transmission over the memory bus based on at least one of the first bank readiness ~~signals~~ or the second bank readiness signal.

8. (Original) The method of claim 7, further comprising:

sending the selected memory transaction over the memory bus.

9. (Original) The method of claim 7, wherein each of the memory transactions is associated with a different priority in a set of priorities, and wherein selecting further comprises:

selecting the one of the memory transactions when the bank readiness signal indicates that the memory bank to which the one of the memory transactions is destined is ready to accept a memory transaction and the priority associated with the one of the memory transactions is greater than a priority associated with any of the other memory transactions.

10. (Original) The method of claim 9, further comprising:

associating the priorities with the memory transactions based on an age of the memory transactions.

11. (Currently Amended) The method of claim 7, wherein generating the first bank readiness signal and generating the second bank readiness signal comprises:

generating the first and second bank readiness signals using a state machine coupled to the memory bus.

12. (Currently Amended) The method of claim 7, wherein generating the first bank readiness signal comprises:

sending ~~a~~ the first one of the plurality of memory ~~transaction~~ transactions to a memory bank;

clearing the bank readiness signal for the memory bank at approximately the time of sending the first one of the plurality of memory ~~transaction~~ transactions to the memory bank; and

setting the bank readiness signal for the memory bank a predetermined period of time after sending the memory first one of the plurality of memory ~~transaction~~ transactions to the memory bank.

13. (Currently Amended) An apparatus comprising:

means for identifying a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks;

means for generating a ~~plurality of bank readiness signals based upon a content of the memory bus, each bank readiness signal generated using an arbiter simultaneously coupled to each of the plurality of memory transactions and indicating the readiness of one of the memory banks to accept a memory transaction;~~ first bank readiness signal by monitoring an address of a first one of the plurality of memory transactions gated across the memory bus at a location along the memory bus, wherein the first bank readiness signal indicates the readiness of one of the memory banks to accept ~~a~~ the first one of the plurality of memory transactions;

means for generating a second bank readiness signal by monitoring an address of a second one of the plurality of memory transactions gated across the memory bus at a location along the memory bus, wherein the second bank readiness signal indicates the readiness of another of the memory banks to accept the second one of the plurality of memory transactions; and

means for selecting a third one of the memory transactions for transmission over the memory bus based on at least one of the first bank readiness ~~signals~~ or the second bank readiness signal.

14. (Original) The apparatus of claim 13, further comprising:

means for sending the selected memory transaction over the memory bus.

15. (Original) The apparatus of claim 13, wherein each of the memory transactions is associated with a different priority in a set of priorities, and wherein means for selecting further comprises:

means for selecting the one of the memory transactions when the bank readiness signal indicates that the memory bank to which the one of the memory transactions is destined is

ready to accept a memory transaction and the priority associated with the one of the memory transactions is greater than a priority associated with any of the other memory transactions.

16. (Original) The apparatus of claim 15, further comprising:

means for associating the priorities with the memory transactions based on an age of the memory transactions.

17. (Previously Presented) The apparatus of claim 13, wherein the content of the memory bus comprises an address of a memory transaction monitored by a state machine.

18. (Original) The apparatus of claim 13, wherein means for generating comprises:

means for sending a memory transaction to a memory bank;

means for clearing the bank readiness signal for the memory bank at approximately the time of sending the memory transaction to the memory bank; and

means for setting the bank readiness signal for the memory bank a predetermined period of time after sending the memory transaction to the memory bank.

19. (Currently Amended) A computer program product, tangibly stored on a computer-readable medium, the product comprising instructions operable to cause a programmable processor to:

identify a plurality of memory transactions to be sent over a memory bus to a memory having a plurality of memory banks, each memory transaction addressed to one of the memory banks and stored in a request station provided in a queue;

generate a plurality of bank readiness signals based upon a content of the memory bus by monitoring the addresses of a first group of the plurality of memory transactions gated across the memory bus at a location along the memory bus, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction; and

select an additional one of the plurality of memory transactions for transmission over the memory bus based on the bank readiness signals.

20. (Previously Presented) The apparatus of claim 13, wherein the plurality of memory transactions are sent over the memory bus one memory transaction at a time.

21.-24. Canceled

25. (Previously Presented) The computer program product of claim 19, wherein the content of the memory bus comprises an address of a memory transaction monitored by a state machine.